100Gb/s CFP2 Optical Transceiver

290-601

Features

- *D C*
- *+3.3*
- *H -*
- *112G*
- *10*
- *AC C*
- *1310 EA-DFB D*
- *I A*
- *(:9)*
- *B*
- *:0℃ 70℃*
- *C H*
- *DI C I*

Application

- *- 4*
-
-
- *A*

Standards

- C IEEE 802.3
- C CF 2 A , 1.0 J 31,2014
- C CF A , 2.2J 01, 2013
- C I - G.959.1
- C H & EEE

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	Ts	°C	-40	+85
Relative Humidity	RH	%	5	85

Output Low Voltage (I_{OL}=100uA)	3.3VOL	V			0.2	
Minimum Pulse Width of Control Pin Signal	t_CNTL	us	100			
1.2V LVCMOS Electrical Characteristics						
Input High Voltage	1.2VIH	V	0.84		1.5	
Input Low Voltage	1.2VIL	V	-0.3		0.36	
Input Leakage Current	1.2IIN	uA	-100		+100	
Output High Voltage	1.2VOH	V	1.0		1.5	
Output Low Voltage	1.2VOL	V	-0.3		0.2	
Output High Current	1.2IOH	mA			-4	
Output Low Current	1.2IOL	mA	+4			
Input Capacitance	Ci	pF			10	
Optical transmitter Characteristics						
Signaling Rate for Each Lane （100GbE）		Gbps	-	25.78125		
Signaling Rate for Each Lane （OTU4）				27.95249		
Four Lane Wavelength Range	1	nm	1294.53	1295.56	1296.59	
	2		1299.02	1300.05	1301.09	
	3		1303.54	1304.58	1305.63	
	4		1308.09	1309.14	1310.19	
Side Mode Suppression Ratio	SMSR	dB	30		-	
Total Average Launch Power	Pt	dBm	-		10.5	
Average Launch Power for Each Lane(100GbE)	Pa	dBm	-4.3		+4.5	2
Average Launch Power for Each Lane(OTU4)			-2.9		+4.5	
Optical Modulation Amplitude for Each Lane	OMA	dBm	-1.3		4.5	3
Transmitter and Dispersion Penalty for Each Lanes		TDP			2.2	
Average Launch Power of Off Transmitter for Each Lanes Extinction Ratio (100GbE)	Poff	dBm	-		-30	

Receiver Sensitivity in OMA for Each Lane(100GbE)	SOMA	dBm		-8.6	8
Receiver Sensitivity in OMA for Each Lane(OTU4)				-10.8	9
Stressed Receiver Sensitivity in OMA for Each Lane		dBm		-6.8	10&11
Los Assert		dBm			-12
Los De-assert		dBm	-17		
Los Hysteresis		dBm		0.2	

Note1. The supply current includes CFP module's supply current and test board working current.

Note2.

Management Interface Pins(MDIO)

The CFP Module supports alarm, control and monitor functions via an MDIO bus. The CFP MDIO pins are listed in the following table: Management Interface Pins

Management Interface Pins

Pin#	Symbol	Description	I/O	Logic	H	L	Pull-up/down
13	GLB_ALRMn	Global Alarm	I	3.3V LVCMOS	Ok	Alarm	
18	MDIO	Management Data Input Output Bi-Directional Data	I/0	1.2V LVCMOS			
17	MDC	MDIO Clock	I	1.2V LVCMOS			
19	PRTADR0	MDIO Physical Port address bit0	I	1.2V LVCMOS	per MDIO document[5]		
20	PRTADR1	MDIO Physical Port address bit1	I	1.2V LVCMOS			
21	PRTADR2	MDIO Physical Port address bit2	I	1.2V LVCMOS			

Hardware Signaling Pin Timing Requirements

Timing Parameters for CFP hardware Signal Pins are listed in the following table.

Timing Parameters for CFP hardware Signal Pins

Parameter	Symbol	Min	Max	Unit	Notes&Conditions
Hardware MOD_LOPWR assert	t_MOD_LOPWR_assert		1	ms	

Time					"OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Global Alarm De-assert Delay Time	GLB_ALRMn_deassert		150	ms	This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details
Management Interface Clock Period	t_prd	250		ns	MDC is 4MHz rate
Host MDIO t_setup	t_setup	10		ns	
Host MDIO t_hold	t_hold	10		ns	
CFP MDIO t_delay	t_delay	0	175	ns	
Initialization time from Reset	t_initialize		2.5	s	
Transmitter Disabled(TX_DIS_asserted)	t_deassert		100	us	Application Specific
Transmitter Enabled(TX_DIS_asserted)	t_assert		20	ms	Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification"

High Speed Electrical Characteristics

Reference Clock Characteristics（optional）

		Min	Typ	Max	Unit	Notes
Impedance	Zd	80	100	120	Ω	

1/

161.1328125/644.53125

Frequency MHz

Differential Voltage		Differential

				Network Lane		
801D	1	RO	7~0	Maximum Power Consumption		
801E	1	RO	7~0	Maximum Power Consumption in Low Power Mode		
801F	1	RO	7~0	Maximum Operating Case Temp Range		
8020	1	RO	7~0	Minimum Operating Case Temp Range		
8021	16	RO	7~0	Vendor Name		
8031	3	RO	7~0	Vendor OUI		
8034	16	RO	7~0	Vendor Part Number		
8044	16	RO	7~0	Vendor Serial Number		
8054	8	RO	7~0	Data Code		
805C	2	RO	7~0	Lot Code		
805E	10	RO	7~0	CLEI Code		
8068	1	RO	7~0	CFP MSA hardware Specification Revision Number		
8069	1	RO	7~0	CFP MSA Management Interface Specification Revision Number		
806A	2	RO	7~0	Module Hardware Version Number		
806C	2	RO	7~0	Module Firmware Version Number		
806E	1	RO	7~0	Digital Diagnostic Monitoring Type		
806F	1	RO	7~0	Digital Diagnostic Monitoring Capability 1		
8070	1	RO	7~0	Digital Diagnostic Monitoring Capability 2		
8071	1	RO	7~0	Module Enhanced Options		
8072	1	RO	7~0	Maximum High-Power-up Time		
8073	1	RO	7~0			

8084	2	RO	7~0	Transceiver Temp Low Warning Threshold			
8086	2	RO	7~0	Transceiver Temp Low Alarm Threshold			
8088	2	RO	7~0	VCC High Alarm Threshold			
808A	2	RO	7~0	VCC High Warning Threshold			

				Select		
			15~8	Reserved		
		RW	7~0	Function Select Code		
A008	1	RO		**PRG_ALRM3Source Select**		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A009	1	RO		**PRG_ALRM2Source Select**		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00A	1	RO		**PRG_ALRM1Source Select**		
			15~8	Reserved		
		RW	7~0	Alarm Source Code		
A00B	1	RO		Module Bi-/Uni-Directional Operating Mode Select		
			15~3	Reserved		
		RW	2~0	Module Bi/uni-Direction Mode Select		
A00C	4	RO		Reserved		

RW	9	RX FIFO Auto Reset

			12	Network Lane Alarm and Warning Summary		
			11	Module Alarm and Warning 2 Summary		
			10	Module Alarm and Warning 1 Summary		
			9	Module Fault Summary		
			8	Module General Status Summary		
			7	Module State Summary		
			6~1	Reserved		
			0	Soft GLB_ALRM Test Status		
A019	1	RO		**Network Lane Alarm and Warning Summary**		
			15	Lane 15 Alarm and Warning Summary		
			14	Lane 14 Alarm and Warning Summary		
			13	Lane 13 Alarm and Warning Summary		
			12	Lane 12 Alarm and Warning Summary		
			11	Lane 11 Alarm and Warning Summary		
			10	Lane 10 Alarm and Warning Summary		
			9	Lane 9 Alarm and Warning Summary		
			8	Lane 8 Alarm and Warning Summary		
			7	Lane 7 Alarm and Warning Summary		
			6	Lane 6 Alarm and Warning Summary		
			5	Lane 5 Alarm and Warning Summary		
			4	Lane 4 Alarm and Warning Summary		
			3	Lane 3 Alarm and Warning Summary		
			2	Lane 2 Alarm and Warning Summary		
			1	Lane 1 Alarm and Warning Summary		
			0	Lane 0 Alarm and Warning Summary		
A01A	1	RO		**Network Lane Fault and Status Summary**		
			15	Lane 15 Fault and Status Summary		
			14	Lane 14 Fault and Status Summary		
			13	Lane 13 Fault and Status Summary		
			12	Lane 12 Fault and Status Summary		
			11	Lane 11 Fault and Status		

				Summary		
			10	Lane 10 Fault and Status Summary		

A01C	1	RO		Reserved		
Module FAWS Registers						
A01D	1	RO		**Module General Status**		
			15	Reserved		
			14	Reserved		
			13	HW_Interlock		
			12~11	Reserved		
			10	Loss of REFCLK Input		
			9	TX_JITTER_PLL_LOL		

		/ / / /	7	TX-Turn-off State Latch		

		RO/LH/COR	3	Mod Aux 2 High Alarm Latch		
		RO/LH/COR	2	Mod Aux 2 High Warning Latch		
		RO/LH/COR	1	Mod Aux 2 Low Warning Latch		
		RO/LH/COR	0	Mod Aux 2 Low Alarm Latch		
A027	1	RO		Reserved		

	8	TX Power Low Alarm		
	7	Laser Temperature High Alarm		
	6	Laser Temperature High Warning		
	5	Laser Temperature Low Warning		
	4	Laser Temperature Low Alarm		
	3	RX Power High Alarm		
	2	RX Power High Warning		
	1	RX Power Low Warning		
	0	RX Power Low Alarm		

RO **ne n Fault and**

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			7	Lane TX_LOSF Latch		
			6	Lane TX_LOL Latch		

A280 16

		RO	15~4	Reserved		
		RW	3~0	Signal Pre/De-emphasis		
A450	48	RO		Reserved		

11	3.3
12	3.3
13	3.3 G D
14	3.3 G D
15	D I A
16	D I B
17	G C 1
18	G C 2
19	G C 3
20	G A 1
21	G A 2
22	G A 3
23	G D
24	DI

94	.C.
93	.C.
92	G D
91	.C.
90	.C.
89	G D
88	1
87	1
86	G D
85	0
84	0
83	G D
82	.C.
81	.C.

48	.C.
49	G D
50	*(RX_MCLKn)*
51	*(RX_MCLKp)*

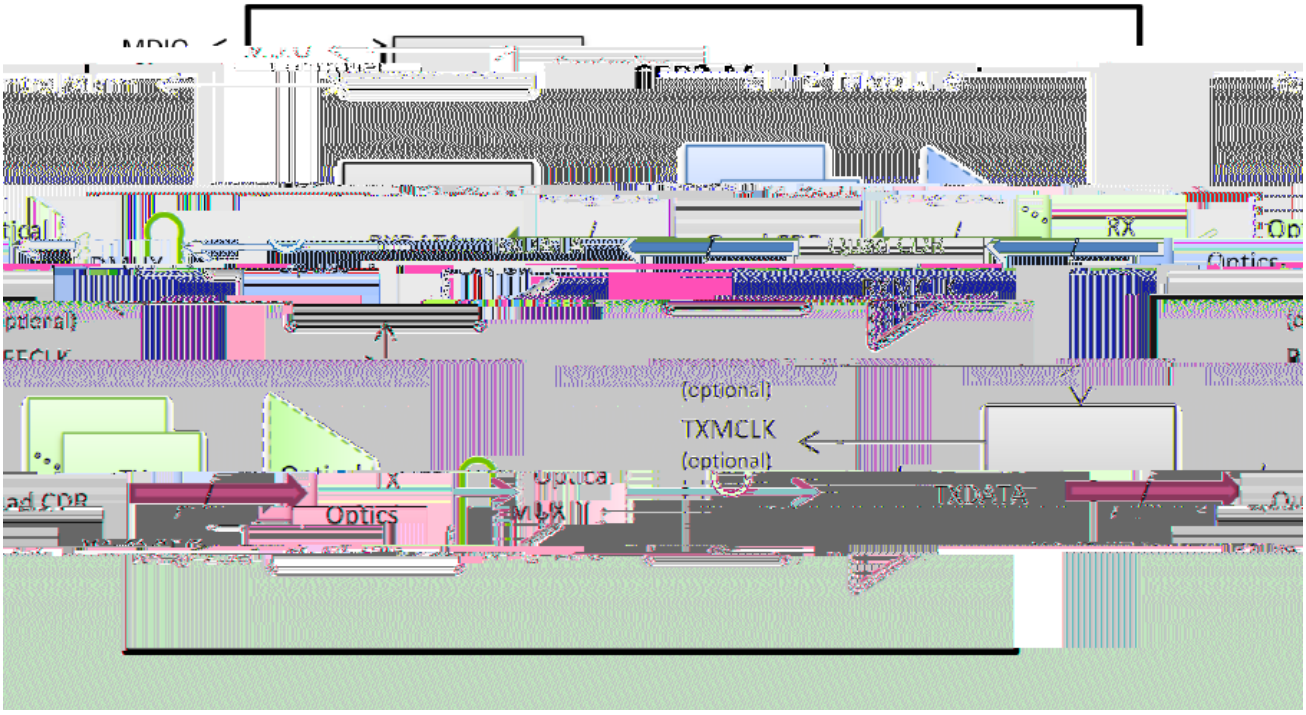
57	0
56	G D
55	.C.
54	□9 92C3)□□9 I76

				," "
26	D □		/	." " ( ) ," " -
27	D AB			." " ," " ,
28	D		/	." " ," " ,
29	G B A			. " ," " , ,
30	G D			
31	DC		.	(. -)
32	DI	/	.	/ - (. -)
33	AD 0		.	
34	AD 1		.	
35	AD 2		.	
36	D I C	/		/ . !
37	D I D	/		/ . !
38	D I E	/		/ . !
39	3.3 G D			
40	3.3 G D			
41	3.3			.
42	3.3			
43	3.3			
44	3.3			
45	3.3 G D			
46	3.3 G D			
47	.C.			
48	.C.			
49	G D			
50	*(RX_MCLKn)*			. .
51	*(RX_MCLKp)*			. .
52	G D			
53	G D			
54	.C.			
55	.C.			
56	G D			
57	0			

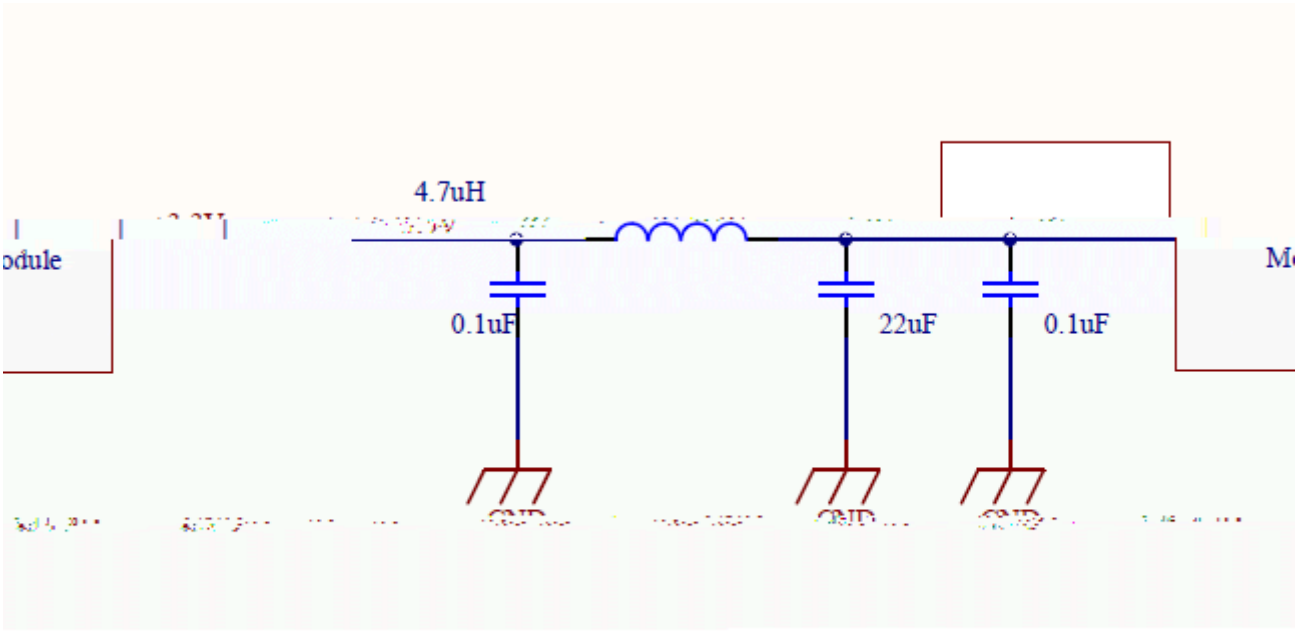
58	0			
59	G D			
60	1			
61	1			
62	G D			
63	.C.			
64	.C.			
65	G D			
66	.C.			
67	.C.			

94	.C.			
95	[redacted]			

Block diagram



Required Host Board Components



Package outline

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7